ALL REG'S CLOCKED ON CLK.20 UNLESS OTHERWISE SPEC'D

*2 DATA INPUTS CLOCK CONDITIONED W/ 10MHZ

*3: 652 PUT IN F/T, AND BOTH PIPE REG'S

SET FOR 1 DELAY TO ALIGN ADDRESS W/DATA
DURING LUT LOAD/READ

*: NUMBERS IN PARENTHESIS ARE FOR RAW READS AND WRITES
CLOCK SKEW RELATIVE TO ORM -7>SKEW<+5

CT

F374

ADDRESS

CLK

ORM

F244

F4

XILINX

SETUP:0NS

HOLD:10NS

AS652

BUFF. DELAY:

2-10NS

CLOCK CIRCUITRY

DELAY: 3-8 NS.

TRACE/CONN/BP.DELAY:8 NS

DOTS

F74 CLK/Q:

3.8-7.8

CT

F74 CLK/Q:

3.8-7.8

MAX CLK/Q: DATA TO DOTS: 5+10+8+9+8:40NS

MAX CLK/Q DELAY TO ORM:+5+7.8+10 NS+6.5==29.3 nSEC

DCK:MAX CLK/Q:54.6 NSEC
ALL REG'S CLOCKED ON CLK.20 UNLESS OTHERWISE SPEC'D
NOTES
1: ALL REG’S CLK’D BY SCLK20 (20 MHZ EN’D CLK) 2: C: CSR (GEN’D INTERNALLY)